1. Processing Units
   1. Description: Two independent FPGA processor units with independent front-end optical links and independent back-end LVDS/GTH connection to motherboard FPGA
   2. FPGA Specifications

* Footprint: 1FFG1158
* Compatible Part Numbers: XC7VX415T, XC7VX485T, XC7VX550T, XC7VX690T

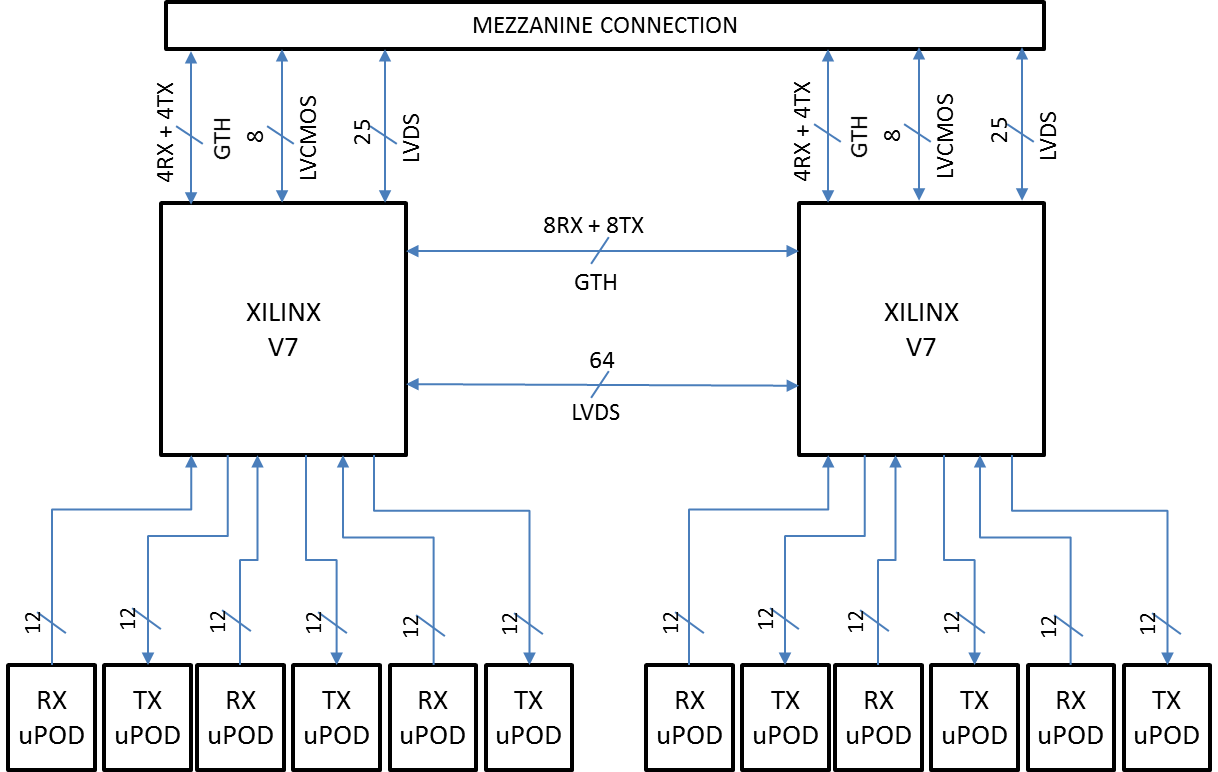


Figure . Diagram of the communication links

1. Communication Links
   1. Front-end Optical Links
      * Optical Transceivers: Avago MicroPOD
      * FPGA Transceivers: GTH bank
      * Number of modules for each FPGA: 3 Rx + 3 TX (36/36 fibers)
      * Number of modules total: 6 Rx + 6 TX (72/72 fibers)
      * Front-end optical connectors:
        + Type: MTP
        + Number of fibers per optical connector: 24 (12 TX + 12 RX)
        + Number of fibers per optical connector (RX only option): 12 RX
        + Total Number of connectors : 6
      * Management: Each FPGA controls its optical modules via I2C bus.
   2. Mezzanine connection

Description: Both FPGAs are connected independently via the mezzanine connector to one FPGA unit on the motherboard. There are 3 types of connections: LVDS, low-speed LVCMOS, GTH.

* + 1. LVDS Connection
       - Number of lines: 25 / each FPGA
       - Protocol: no protocol assumed. Each line can be used in any direction or bidirectional
    2. LVCMOS Connection
       - Number of lines: 8 / each FPGA
       - Protocol: no protocol assumed. Each line can be used in any direction or bidirectional
    3. GTH Connection
       - Number of lines: 4RX+4TX / each FPGA
       - Protocol: no protocol assumed.
  1. Inter-FPGA connection
     1. LVDS Connection
        + Number of lines: 64
        + Protocol: no protocol assumed. Each line can be used in any direction or bidirectional
     2. GTH Connection
        + Number of lines: 8RX+8TX
        + Protocol: no protocol assumed.

1. Clock Distribution
   1. Mezzanine Clock sources (from Carrier)
      1. Mezzanine System Clock

System clock is generated on the carrier motherboard by a 0-delay PLL (LMK03200) from either an external source (via RTM or AXIe backplane) or from a local oscillator

* + - * Sources
        + Local Oscillator
        + RTM
        + Backplane (AXIe standard)
    1. Mezzanine GTH Clock
       - A separate clock is generated by the same PLL circuit as the system clock.
       - In upcoming upgrade of the motherboard, the two clock paths will use two independent PLL circuits

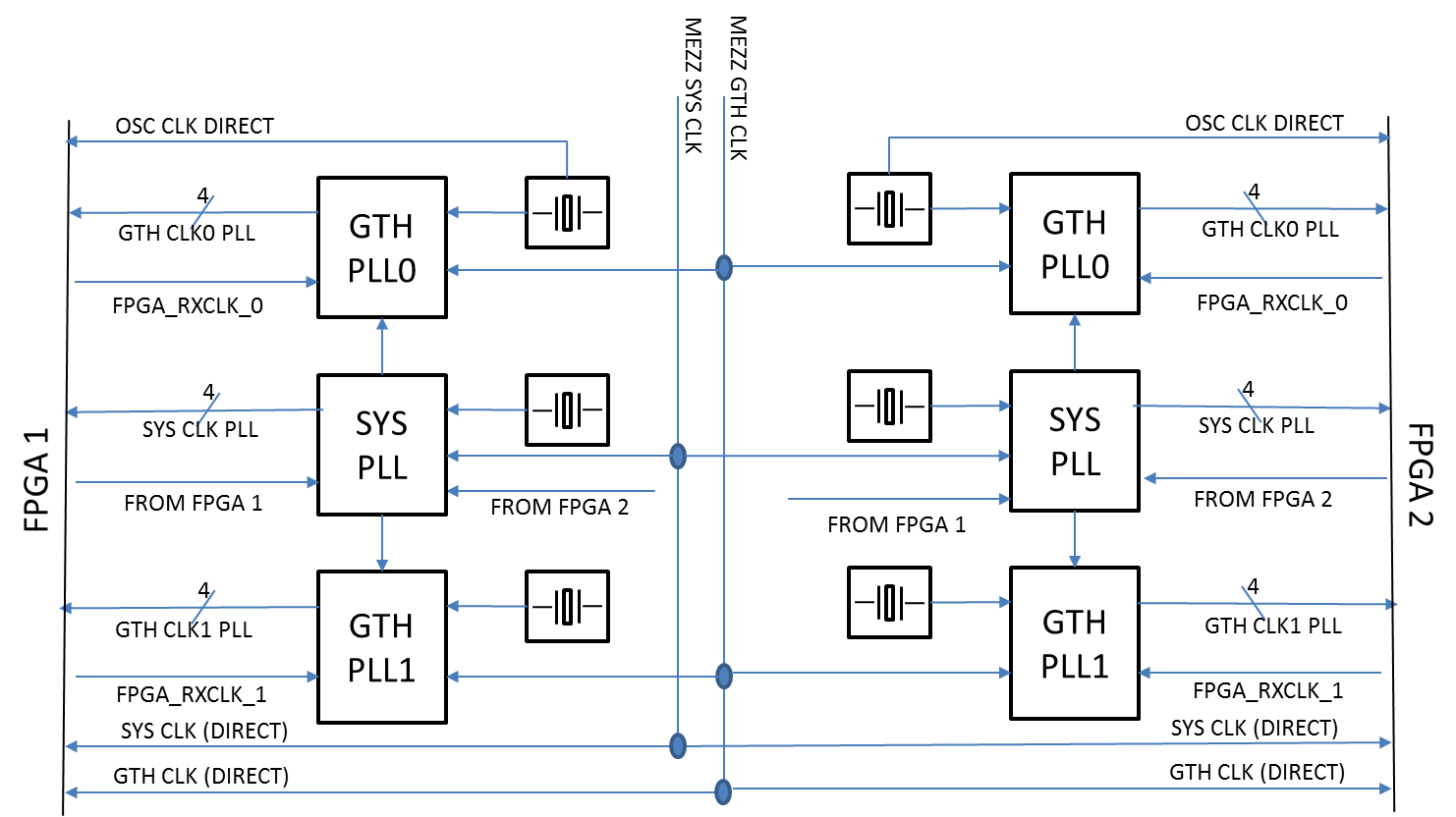


Figure . Diagram of the Clock Distribution scheme.

* 1. Clock conditioners

Description: Each FPGA system has its own dedicated clock distribution tree, consisting of one 0-delay PLL for the system clock and 2 PLLs for the serializers clock references. The two clock sources (system and GTH reference) originates from the carrier motherboard. Optionally, the source can be switched to dedicated local crystal oscillators or clock outputs from the FPGA (i.e. recovered from incoming optical links).

The purpose of a second PLL for the GTH reference clocks is to be able to implement two independent protocols in the processing unit.

* + 1. System-Clock PLL
       - Purpose: Jitter cleaner, synthesizer or 0-delay buffer for the system clock
       - Type: LMK03200
       - Sources:
         * Mezzanine System Clock
         * Local Oscillator 0
         * FPGA processor 0
         * FPGA processor 1
       - Outputs:
         * FPGA (4 outputs)
         * GTH-Clock PLL 1 (1 output)
         * GTH-Clock PLL 2 (1 output)
    2. GTH Clock PLL 1
       - Purpose: Jitter cleaner, synthesizer for GTH clock reference
       - Type: LMK03806
       - Sources:
         * Mezzanine GTH Clock
         * Local Oscillator 1
         * FPGA recovered clock
         * PLL 0 (derived from system clock)
       - Outputs:
         * FPGA GTH REFCLK (4 outputs)
    3. GTH Clock PLL 2
       - Purpose: Additional jitter cleaner, synthesizer for GTH clock reference
       - Type: LMK03806
       - Sources:
         * Mezzanine GTH Clock
         * Local Oscillator 1
         * FPGA recovered clock
         * PLL 0 (derived from system clock)
       - Outputs:
         * FPGA GTH REFCLK (4 outputs)
    4. Direct clock connections to FPGA processing unit (start-up clocks)
       - System Clock from carrier
       - GTH Clock from carrier
       - Local Oscillator 0
    5. Management
       - All 3 PLLs are in direct control of the FPGA processing unit

1. Power Distribution
   1. Power sources
      1. 12V power originates from the carrier board (ATCA supply chain)
      2. Optional 12V connector, for benchtop operation
   2. Separate power conditioners
      1. The two FPGA have separate power distribution circuits
         * 1.0V@20A : core and BRAM
         * 1.8V@1A : VAUX and IO
         * 1.8V@1A : MGT VCC
         * 1.0V@10A : MGT AVCC
         * 1.2V@4A : MGT AVTT
   3. Common power conditioners
      * + [3.3V@4A](mailto:3.3V@4A) : optical modules
        + [3.3V@4A](mailto:3.3V@4A) : PLLs
        + [2.5V@6A](mailto:2.5V@6A) : optical modules
   4. Total Power Rating:
      1. Power Output: 120W
      2. Power Input : 150W
   5. Power Management
      * + All power circuits are controlled by an IPMC microprocessor unit which is connected to the IPMI bus of the carrier board
        + Sequencer circuits for the 2 FPGA power domains
        + Phase control circuit for the DC/DC converters
2. Board Management
   1. IPMI Bus

The local IPMI bus is connected to the IPMI bus of the carrier board via the mezzanine connector

* + 1. IPMC Microcontroller
       - Inputs
         * Power monitors of the local DC/DC converters
         * Temperature sensors
       - Outputs
         * Power enable for the two FPGA processing units (independent)
         * Reset signals for the two FPGA (independent)
       - IPMI bridge
         * IPMI bus for the two FPGA
       - Auxiliary control
         * RS232 for debug/benchtop operation
    2. FPGA Emulated IPMC
       - The IPMI bus is bridged by the IPMC Microcontroller to the two FPGA units
       - Emulated IPMC can be used to control processor parameters (i.e. PLL settings, power status, temperature)

